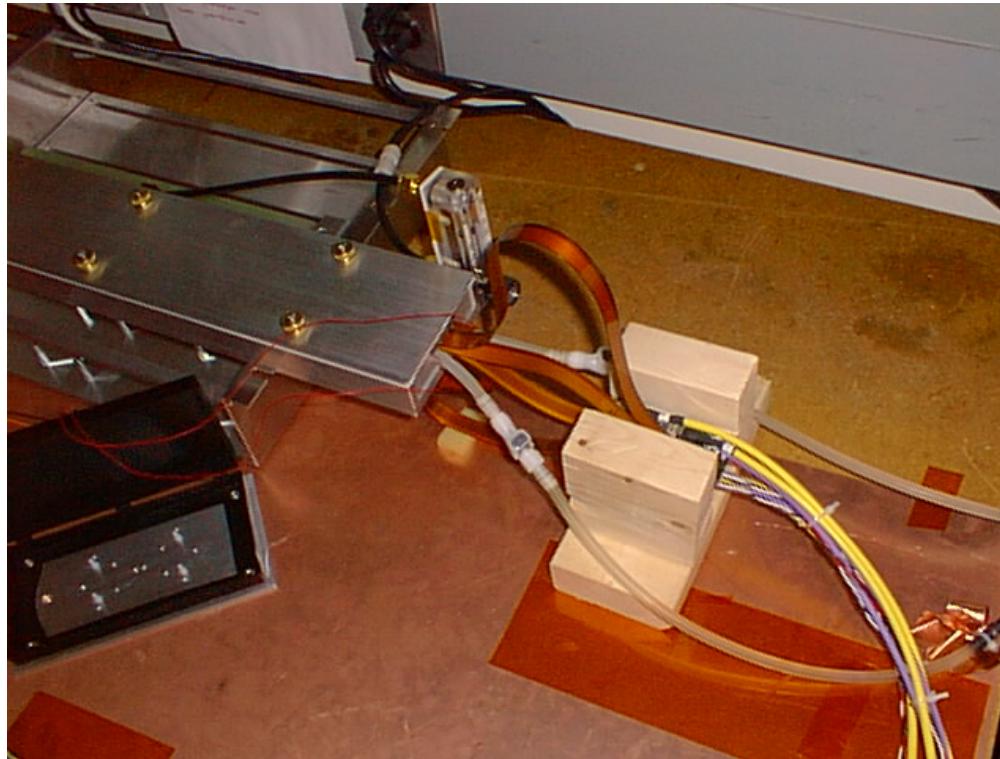


# Layer 2 Stave Readout Results



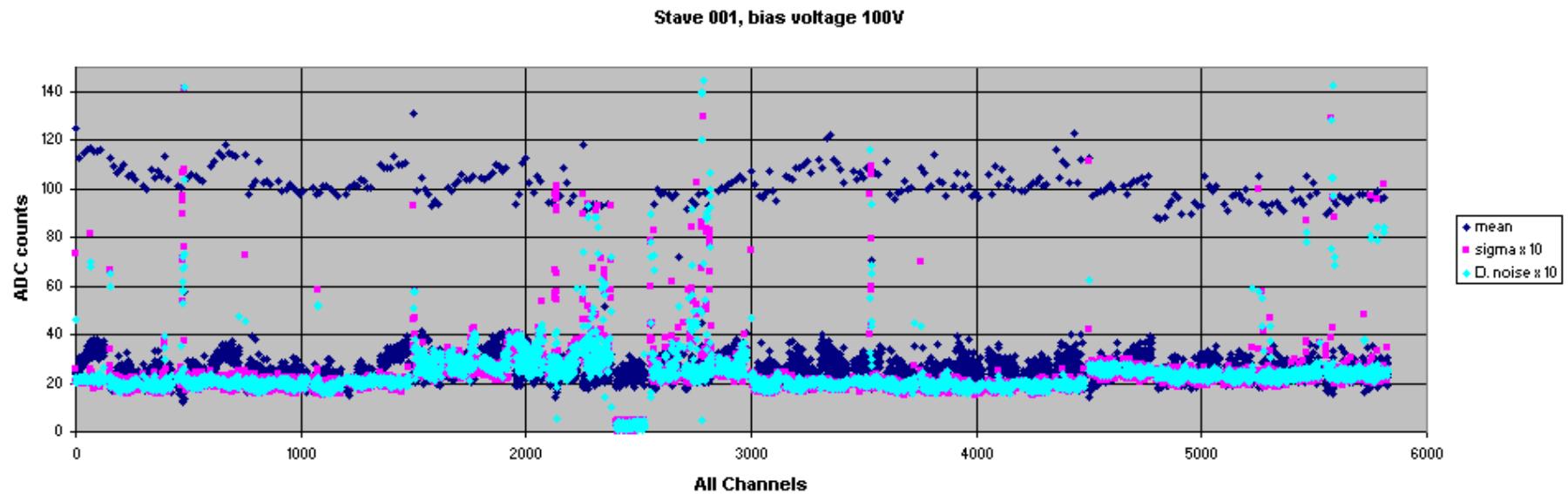
## Test stand setup

- ★ stave in metal case with dry air and liquid cooling
- ★ full chain readout revision 2, including HV
- ★ 2 SaSeqs — master and slave
- ★ very latest (last?) spreadsheet
  - based on Gustavo's spreadsheet 2.7
  - additional debug options
  - sparse mode readout for old and new SVX4 revisions
  - improved download (works perfectly with 4 hybrids)

## Readout parameters

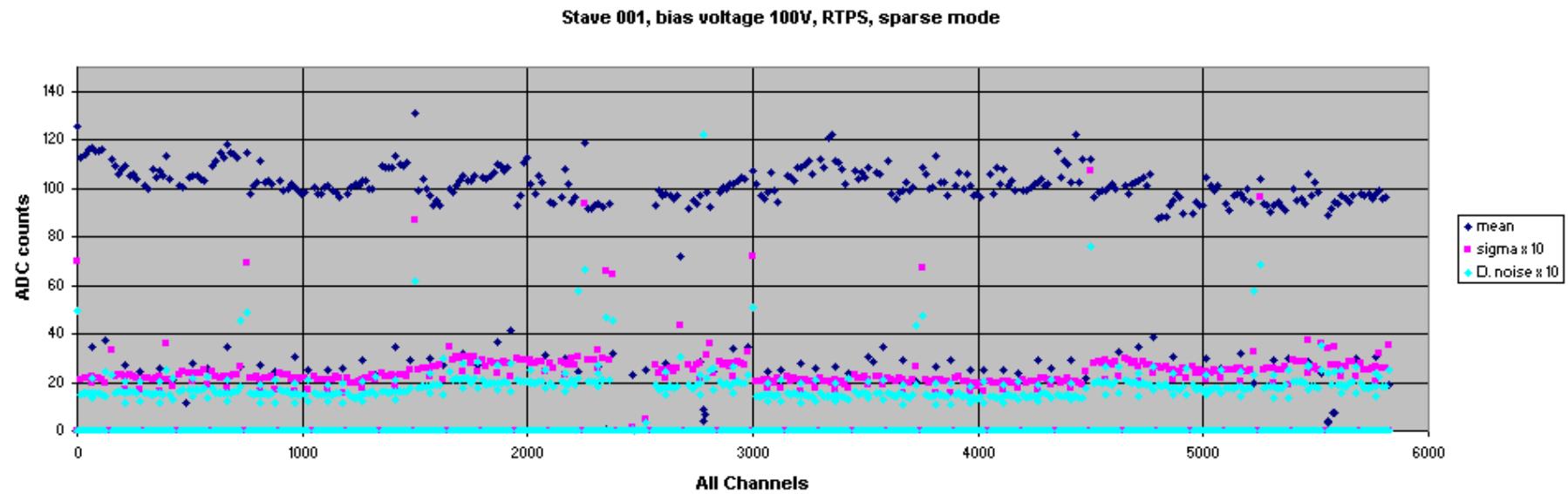
- ★ sensor bias voltage 100V
- ★ dynamic pedestal subtraction
- ★ pipeline 8
- ★ calinject mode — every 16th channel
- ★ VME bus: DMA data transfer (60–100 events/s)

## Results: read all mode



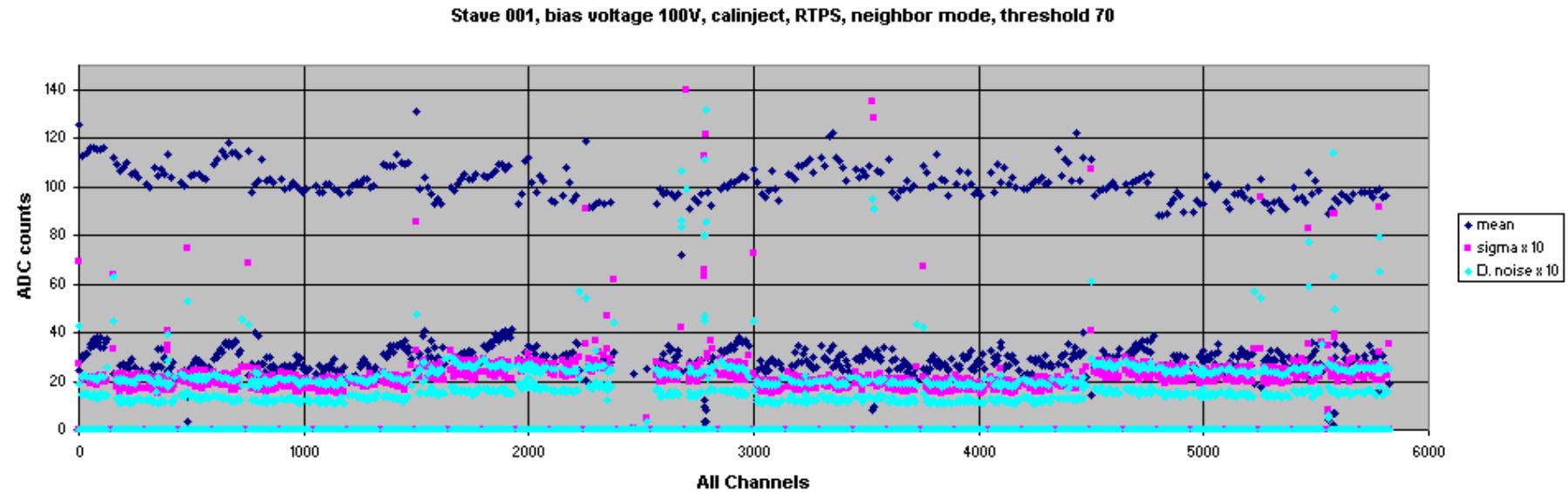
20-20S module misbehaves a bit (worse without HV bias)

# Results: sparsified mode



threshold at 70 ADC counts

## Results: neighbor mode



errors seen in one million events:

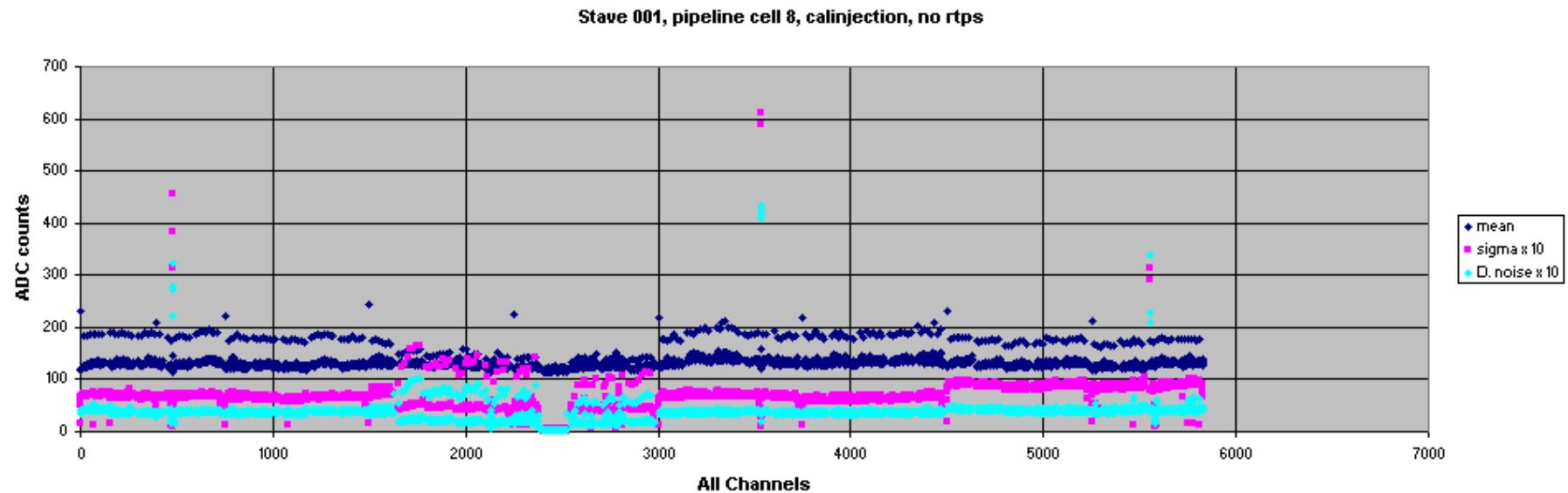
4 DMA errors

(VME communication failure SaSeq-Bit3, no problem)

1 real error

(3 chips of 20-20S read 0 ADC counts in most channels)

# Remaining (minor!) readout problems



This plot without HV, without RTPS

- ★ bad calinjection in second module (20-20S)
- ★ one bad chip (20-20S)
- ★ one chip bypassed in last module (20-20A)
- ★ common mode noise
- ★ a few pinholes
- ★ 10-10A (3rd in plot) draws  $80\mu\text{A}$  at 100V

First electrical stave not perfect,  
but EXCELLENT!  
Thanks to all contributors!

